Notice of Allowability	Application No.	Applicant(s)	
	10/626,149	STANLEY, GERALD R.	
	Examiner	Art Unit	
	Y. J. Han	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *a restriction requirement filed on 7/22/05*.

2. ☒ The allowed claim(s) is/are *1-39 and 47-55*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 11/15/04, 7/24/03
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

J. Han

JESSICA HAN
PRIMARY EXAMINER

DETAILED ACTION

Election/Restrictions

1. This application is in condition for allowance except for the presence of claims 40-46 to Species non-elected without traverse. Accordingly, claims 40-46 been cancelled.

Allowable Subject Matter

1. Claims 1-49 and 47-55 are allowed.

2. The following is an examiner's statement of reasons for allowance:

Claim 1 recites, inter alia, a first boost sub-circuit coupled with a second boost sub-circuit; a second boost converter coupled in series with the first boost converter, where the second boost converter includes a third boost sub-circuit coupled with a fourth boost sub-circuit, where the first and second boost converters are configured to receive an input voltage and supply a boost voltage; and a power factor correction controller coupled with the first and second boost converters, where the power factor correction controller is configured to control the first and second boost converters with interleave as a function of the boost voltage.

Claim 8 recites, inter alia, an input stage power converter that includes at least four boost switches coupled in series, the at least four boost switches configured to be coupled in parallel with an input voltage; and a power factor correction controller coupled with the at least four boost switches, the power factor correction controller configured to direct the at least four boost switches independently with interleave to provide a DC boost voltage from the input voltage, where the power factor correction controller is configured with feedforward control to direct the at least four boost switches as a function of the DC boost voltage.

Claim 19 recites, inter alia, an input stage power converter that includes a power factor correction controller and a first boost converter coupled in series with a second boost converter, where the first and second boost converters are controlled with interleave by the power factor correction controller to supply a DC boost voltage and to control a wave shape of an AC input current supplyable to the power factor correcting power supply by a power source; and an output stage power converter coupled with the first and second boost converters, where the output stage power converter is configured to balance the boost voltage supplied with the first and second boost converters.

Claim 28 recites, inter alia, an input stage power converter that includes a first pair of boost switches coupled in series and a second pair of boost switches coupled in series, where the first and the second pair of boost switches are coupled in series; means for controlling power factor coupled with the first and the second pair of boost switches, the means for controlling power factor configured to control each of the first and the second pair of boost switches with interleave to provide a portion of a boost voltage; and an output stage power converter coupled with the input stage power converter, where the output stage power converter includes a first output converter coupled with the first pair of boost switches and a second output converter coupled with the second pair of boost switches, where the output stage power converter is configured to substantially balance the portion of the boost voltage provided by each of the first and the second pair of boost switches.

Claim 34 recites, inter alia, a first boost switch and a second boost switch, the first and second boost switches coupled in series and configured to be coupled in parallel with an AC power source; a first boost sub-switch coupled in series with the first boost switch; a second

boost sub-switch coupled in series with the second boost switch; a boost capacitor coupled across at least one of the first boost switch coupled in series with the first boost sub-switch and the second boost switch coupled in series with the second boost sub-switch; and a power factor correction controller coupled with the first and second boost switches and the first and second boost sub-switches, where the first and second boost switches and the first and second boost sub-switches are switchable to develop at least a portion of a DC boost voltage on the boost capacitor from an AC input voltage supplyable from the AC power source.

Claim 47 recites, inter alia, providing an power source having an input voltage and an input current; interleave switching at least four boost switches that are coupled in series across the power source to convert the input voltage to a first DC voltage; converting the first DC voltage to a second DC voltage with an output stage power converter; and supplying the second DC voltage to a power rail to supply a load.

The art of record does not disclose the above limitations, nor would it be obvious to modify the art of record so as to include either of the above limitations.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Y. J. Han whose telephone number is 571-272-2078. The examiner can normally be reached on Mon-Fri 5:30am-2:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on 571-272-2084. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

J. Han
Primary Examiner
Art Unit 2838